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Novel Shannon Based Full Adder Architecture Low Power Nueral Network Applications

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Abstract: This paper proposes novel low power full adder cell to be used as Shannon adder in the Neural Network applications. By using the Shannon's theorem the gate count is reduced thereby the total chip area gets minimized. Hence the power also gets reduced to a considerable amount. The designs are implemented using TANNER tool which results in significant reduction in area & power for the Modified Shannon based full adder cell when compared with MCIT based full adder cell.

***Keywords*— Full Adder, Datapath, Shannon's technique, power, Gate count, Area**.

INTRODUCTION:

In state of the art consumer electronics power optimization is an important challenge in VLSI circuits. The battery operated portable devices continues to grow. The traditional approaches for designing these systems vary according to the need of low power design. The power minimization is one of primary design constraint for current day Very Large Scale Integration (VLSI) systems [2]. Datapath/Arithmetic unit forms the heart of most of the state of the art Systems [3]. Hence optimizing the Datapath unit is one of the hot topic of research in the present day VLSI Domain [4].

The artificial neurons or nodes form the neural networks. The Artificial neural networks are formed by connecting artificial neurons (similar to the properties of biological neurons). An artificial neural network involves a network of simple processing elements. Complex systems can be built by connecting the neurons in order to achieve the required functionality.

The layered technique is used to connect neurons. The output of the first layer neurons forms the input to the next layer neurons. The primary inputs of the system will drive the first neuron layer. These neurons are used as buffer (to hold the input values). The next layer is called a hidden layer (since it is invisible to the user). The neurons themselves consists of a set of inputs from the first (input) layer, an implementation of a mathematical function of those inputs, then an output that carries the result of the function to the next layer. This next layer can potentially be another layer whose neurons are now functions of the outputs of the previous layer. After the final hidden layer, a last layer, called the output layer, actually supplies the predicted output values to the user. The self-organizing neural networks are capable of designing themselves. The initialization of a network to perform a specific task is called training. During training the hidden neurons are where the training actually occurs. Every input combination must be tested to see its effects on the output of the system. A comparison between the input and output results in a weight or coefficient that is associated with that input value.

SHANNON THEOREM:

The Shannon Theorem can be categorized as the function of many variables, f (b0, b1, b2, y, bi, y, bn) can be written as the sum of two terms, say one with a particular variable ai, set to 0, and one with it set to 1.

f (b0, b1, b2, ..., bi,.....y, bn) = bi'f (b0, b1, b2, ..., 0,.....y, bn) + bi f (b0, b1, b2, ..., 1,.....y, bn) (1)

EXISTING ARCHITECTURE:

A. Multiplexing Control Input Technique (MCIT):

Based up on the Karnaugh map the MCIT technique is developed. The truth table for full adder is derived from the Boolean expressions for the sum and carry signals. The Boolean expressions are:

C= AB + BC + CA (2)

S= ABC + A'B'C + AB'C' + A'BC' (3)

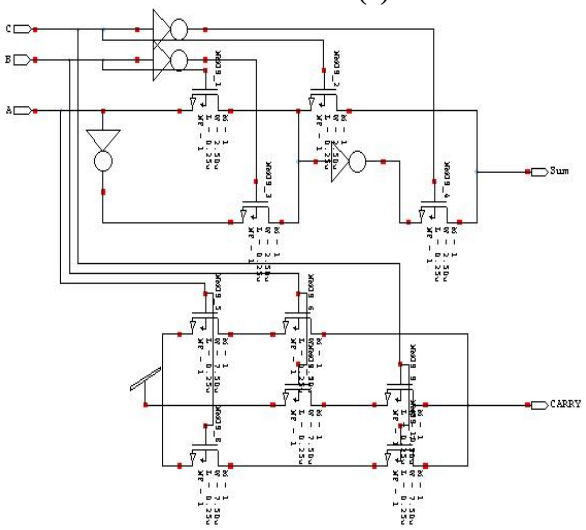

Fig. 1 Shannon based adder using pass transistor logic

B. Existing Shannon Based Full Adder Cell: Reffering to [7], the existing full adder was designed based by combining the MCIT technique for sum and Shannon operation for carry.

Proposed Architecture: Fig 2 shows the proposed full adder circuit for power optimization.

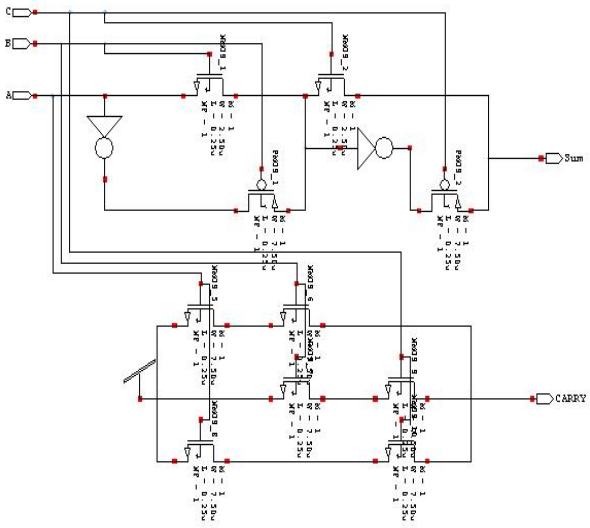

Fig 2. Proposed Full Adder circuit

The proposed low power full adder consists of both PMOS & NMOS transistors. There are no inverters as they are completely eliminated. The innovation is in eliminating the power hungry inverters. The NMOS transistors that require inversion of gate input has been replaced by PMOS transistors.

RESULTS AND ANALYSIS

The existing & proposed architectures are implemented using Full Custom ASIC design methodologies. Both the existing & proposed full adder architectures were simulated using Tanner tool which are mapped to TSMC 250 nm technology node.

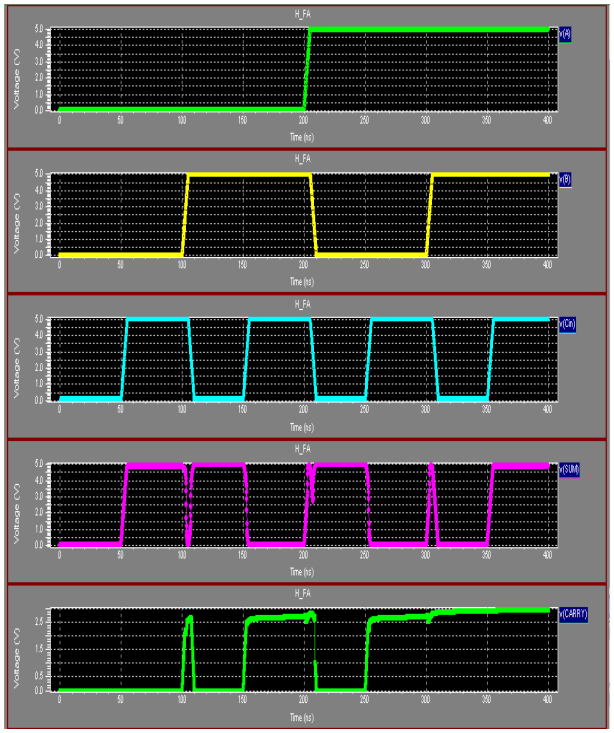

Fig 3: Full Adder wavrforms

Module	*Existing Architecture*	*Proposed Architecture*	*Percentage Gain*
Full Adder	A = 18 T = { A to sum = 227.73 A to carry = 305.00} P = 926.96	A = 14 T = { A to sum = 227.69 A to carry = 305.00} P = 853.991	A = 22 P = 8

Table I: ASIC benchmarking results

Note:

A = Area in Transistor counts.
T = Delay in ns.
P = Power in nW.

The Table I shows the benchmarking results of the existing & proposed architectures after implementing using ASIC design methodology. As depicted in Table I the proposed architecture is well suited for area optimized applications and the performance of the proposed architecture is also unaffected. From Table I, it is clear that the proposed architecture out performs the existing architecture in all the design aspects (Area & Power). It is interesting to note that power has been reduced. Since it is an architectural innovation, below are the low power advantages:

- No Area or Performance penalty.
- Minimum Verification effort:
  - Since it is correct by design.
- It is pervasive:
  - It is independent of adder width.

CONCLUSION

The proposed modified Shannon based full adder cell has been simulated and results are compared with existing Shannon based full adder cell in terms of power, transistor count, timing. This proposed adder cell is having improvement in power & transistor count aspects. The proposed low power concept is proven in both ASIC Design Methodologies.

FUTURE WORK:

In the future work the proposed adder will be used to implement Neural Network. Since adder forms the basic Datapath component in the Neural Network. The proposed low power concept will result in the power optimization during both training of the network & normal functioning of the Neural Network. The plan is to develop a servo motor speed control logic based up on Artificial Neural Network.

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